# ne<mark>x</mark>peria

#### Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <u>http://www.nxp.com</u>, <u>http://www.philips.com/</u> or <u>http://www.semiconductors.philips.com/</u>, use <u>http://www.nexperia.com</u>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © Nexperia B.V. (year). All rights reserved.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

N-channel TrenchMOS SiliconMAX standard level FET

Rev. 04 — 16 November 2009

**Product data sheet** 

### 1. Product profile

### **1.1 General description**

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

Switched-mode power supplies

### 1.4 Quick reference data

Table 1.	Quick reference					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	150	V
		$T_{mb} = 25 \text{ °C}; \text{ see } Figure 1 \text{ and } 2$	-	-	50	
			-	-	-	
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 3</u>	-	-	-	W
Dynamic	characteristics					
$Q_{GD}$	gate-drain charge	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 120 V; T <sub>j</sub> = 25 °C; see <u>Figure 13</u>	-	33	45	nC
Static ch	aracteristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see <u>Figure 11</u> and <u>12</u>	-	30	35	mΩ



### N-channel TrenchMOS SiliconMAX standard level FET

## 2. Pinning information

Table 2.	Pinning	information				
Pin	Symbol	Description	Simplified outline	Graphic symbol		
1	G	gate		-		
2	D	drain	mb			
3	S	source				
mb	D	mounting base; connected to drain		mbb076 S		

# SOT78 (TO-220AB)

## 3. Ordering information

### Table 3.Ordering information

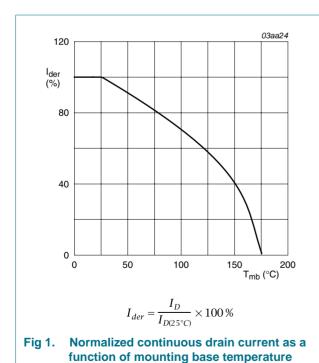
Type number	Package		
	Name	Description	Version
PSMN035-150P	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

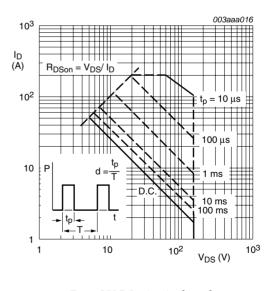
### 4. Limiting values

#### Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	150	V
V <sub>DGR</sub>	drain-gate voltage	$T_j \le 175 \text{ °C}; T_j \ge 25 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$	-	150	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	$T_{mb} = 100 \text{ °C}$ ; see <u>Figure 1</u> and <u>2</u>	-	36	А
		$T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{2} \text{ and } \frac{2}{2}$	-	50	А
I <sub>DM</sub>	peak drain current	$t_p \le 10 \ \mu s$ ; pulsed; $T_{mb} = 25 \ ^{\circ}C$ ; see Figure 2	-	200	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 3</u>	-	250	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-dr	ain diode				
ls	source current	T <sub>mb</sub> = 25 °C	-	50	А
I <sub>SM</sub>	peak source current	$t_p \le 10 \ \mu s$ ; pulsed; $T_{mb} = 25 \ ^{\circ}C$	-	200	А
Avalanche	e ruggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$\label{eq:VGS} \begin{array}{l} V_{GS} = 10 \text{ V};  T_{j(init)} = 25 ^{\circ}\text{C};  \text{I}_{D} = 47  \text{A};  \text{V}_{sup} \leq 50  \text{V}; \\ \text{unclamped};  \text{t}_{p} = 0.1  \text{ms};  \text{R}_{GS} = 50  \Omega; \text{ see } \overline{\text{Figure 4}} \end{array}$	-	460	mJ
I <sub>AS</sub>	non-repetitive avalanche current	$V_{sup} \le 50 \text{ V}; V_{GS} = 10 \text{ V}; T_{j(init)} = 25 \text{ °C}; R_{GS} = 50 \Omega; unclamped; see Figure 4$	-	50	A

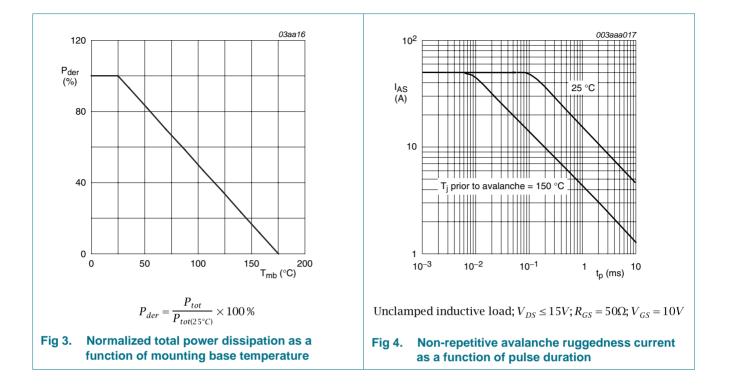




 $T_{mb} = 25^{\circ}C; I_{DM}$  is single pulse

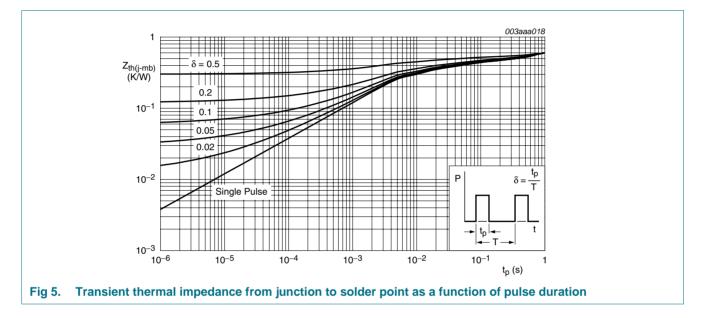


PSMN035-150P\_4



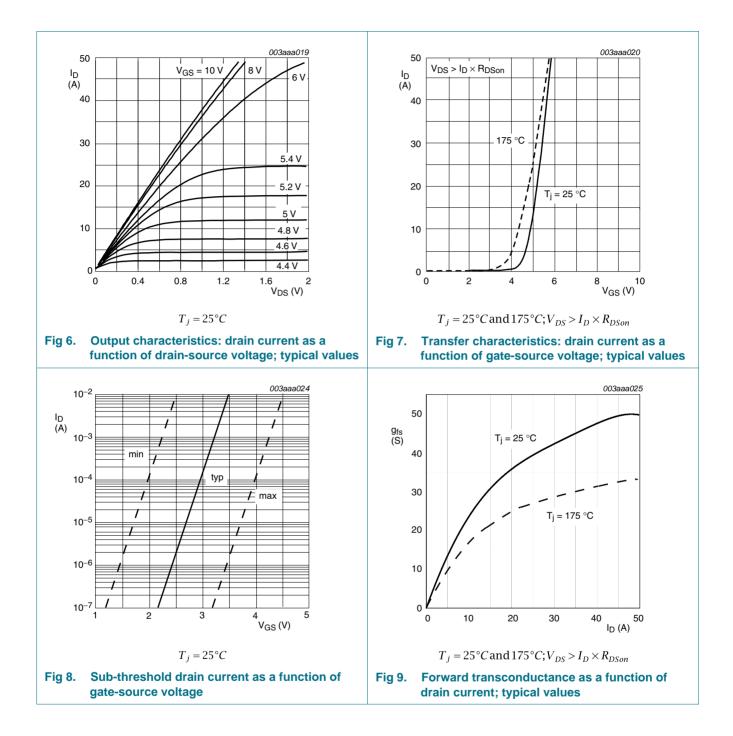
### 5. Thermal characteristics

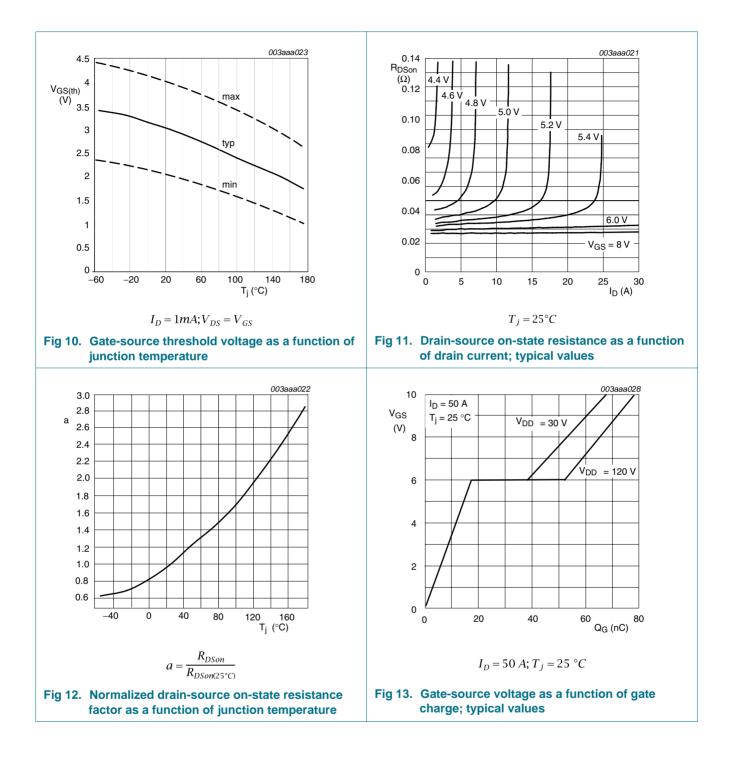
Table 5.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	see Figure 5	-	0.6	-	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	vertical in still air	-	-	60	K/W

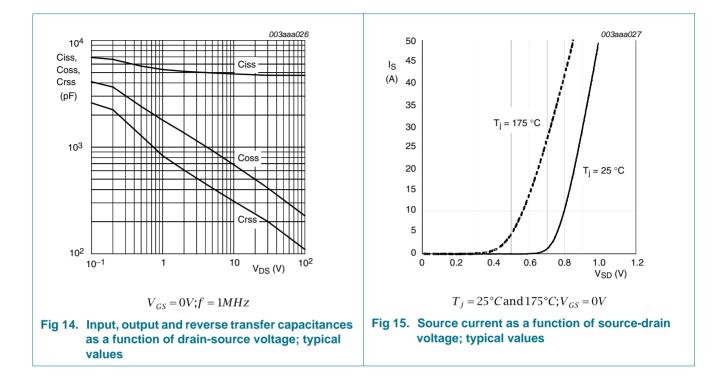


### 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	150	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; see <u>Figure 10</u>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see <u>Figure 10</u>	2	3	4	V
I <sub>DSS</sub>	drain leakage current	$V_{DS}$ = 150 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C	-	0.05	10	μA
		$V_{DS}$ = 150 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = 10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
		$V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; see <u>Figure 11</u> and <u>12</u>	-	-	98	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <u>Figure 11</u> and <u>12</u>	-	30	35	mΩ
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 50 \text{ A}; V_{DS} = 120 \text{ V}; V_{GS} = 10 \text{ V};$	-	79	-	nC
Q <sub>GS</sub>	gate-source charge	$T_j = 25 \text{ °C}; \text{ see } Figure 13$	-	17	-	nC
Q <sub>GD</sub>	gate-drain charge		-	33	45	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	4720	-	pF
C <sub>oss</sub>	output capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	456	-	pF
C <sub>rss</sub>	reverse transfer capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 13</u>	-	208	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 75 V; $R_L$ = 1.5 $\Omega$ ; $V_{GS}$ = 10 V;	-	25	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5.6 \ \Omega; \ T_j = 25 \ ^{\circ}C$	-	138	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	79	-	ns
t <sub>f</sub>	fall time		-	93	-	ns
Source-d	rain diode					
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <u>Figure 15</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}; \text{ d}I_S/\text{d}t = -100 \text{ A}/\mu\text{s}; \text{ V}_{GS} = 0 \text{ V};$	-	118	-	ns
Qr	recovered charge	V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C	-	0.66	-	nC

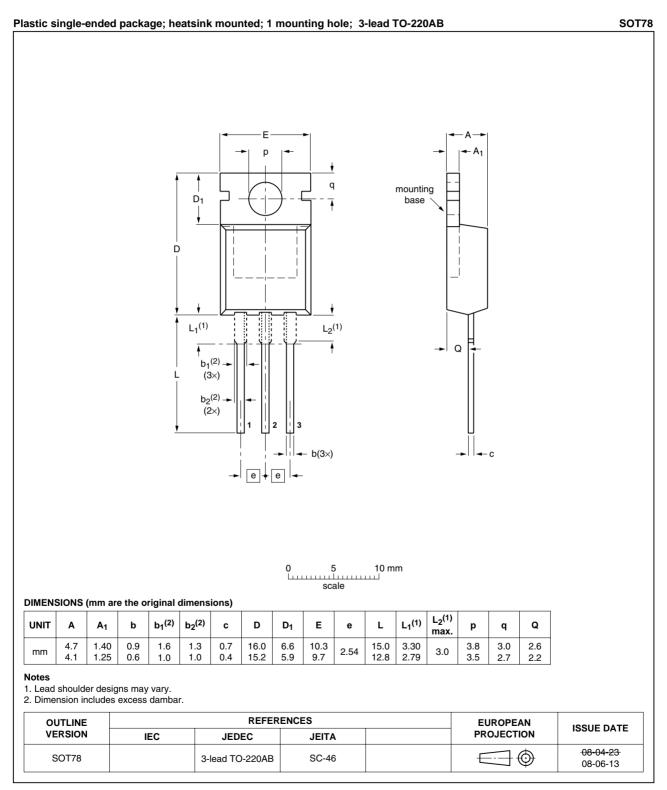






### N-channel TrenchMOS SiliconMAX standard level FET

### 7. Package outline



### Fig 16. Package outline SOT78 (TO-220AB)

## 8. Revision history

Table 7.         Revision history				
Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN035-150P_4	20091116	Product data sheet	-	PSMN035-150_SERIES_HG_3
Modifications:		t of this data sheet has b of NXP Semiconductors	•	o comply with the new identity
	<ul> <li>Legal texts</li> </ul>	s have been adapted to t	he new company	name where appropriate.
	••	ber PSMN035-150P sep -150_SERIES_HG_3.	arated from data s	sheet
PSMN035-150_SERIES_HG_3	20000328	Product specification	-	PSMN035-150_SERIES_2
PSMN035-150_SERIES_2	19990801	Product specification	-	PSMN035-150_SERIES_1
PSMN035-150_SERIES_1	19990201	Objective specification	-	-

### 9. Legal information

### 9.1 Data sheet status

Document status [1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions"

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

### 9.2 **Definitions**

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 9.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

# **Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nxp.com/profile/terms">http://www.nxp.com/profile/terms</a>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

### 9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**TrenchMOS** — is a trademark of NXP B.V.

### **10. Contact information**

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: <a href="mailto:salesaddresses@nxp.com">salesaddresses@nxp.com</a>

### N-channel TrenchMOS SiliconMAX standard level FET

### 11. Contents

1	Product profile1
1.1	General description1
1.2	Features and benefits1
1.3	Applications1
1.4	Quick reference data1
2	Pinning information2
3	Ordering information2
4	Limiting values3
5	Thermal characteristics5
6	Characteristics6
7	Package outline10
8	Revision history11
9	Legal information12
9.1	Data sheet status12
9.2	Definitions12
9.3	Disclaimers
9.4	Trademarks12
10	Contact information12

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

#### © NXP B.V. 2009.

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 16 November 2009 Document identifier: PSMN035-150P\_4

All rights reserved.

